Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("6236222").PN.	US-PGPUB; USPAT	OR	OFF	2005/06/07 15:21
L2	2753	438/14,17,18.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/07 15:35
L3	2530	2 and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/06/07 15:27
L6	95	3 and SOI	US-PGPUB; USPAT	OR	ON	2005/06/07 15:27
L7	1025	324/71.1.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/07 15:27
L8	674	7 and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/06/07 15:36
L10	2420	257/300,350,368.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/07 15:33
L11	2241	10 and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/06/07 15:33
L12	9	11 and (TMAH or tetramethylammonium)	US-PGPUB; USPAT	OR	ON	2005/06/07 15:36
L13	610	11 and (SOI or (silicon adj on adj insulator))	US-PGPUB; USPAT	OR	ON	2005/06/07 15:36
L14	2036	438/149,479,517.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/07 15:36
L15	1798	14 and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/06/07 15:40
L16	620	15 and (SOI or (silicon adj on adj insulator))	US-PGPUB; USPAT	OR	ON	2005/06/07 15:36
L17	11	16 and (TMAH or tetramethylammonium)	US-PGPUB; USPAT	OR	ON	2005/06/07 15:39
L18	0	17 and (secondary adj (electrons or emission))	US-PGPUB; USPAT	OR	ON	2005/06/07 15:40
L19	628	(TMAH or tetramethylammonium) and (SOI or (silicon adj on adj insulator))	US-PGPUB; USPAT	OR	ON	2005/06/07 15:40
L20	507	19 and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/06/07 15:40
L21	0	20 and (secondary adj (electrons or emission))	US-PGPUB; USPAT	OR	ON	2005/06/07 15:40
L22	34	(TMAH or tetramethylammonium) and (SOI or (silicon adj on adj insulator))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 15:40

L23	0	22 and (secondary adj (electrons or emission))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 15:40

US-PAT-NO: 6194253

DOCUMENT-IDENTIFIER: US 6194253 B1

TITLE: Method for fabrication of silicon on insulator substrates

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Brief Summary Text - BSTX (4):
Silicon on insulator (**SOI**) technology oilers many advantages over conventional bulk silicon technology. Among these is the ability to build high performance, high speed. low power complementary-metal-oxide-semiconductor (CMOS) devices.

Drawing Description Text - DRTX (3):
FIGS. 1 to 12 are partial cross-sectional views illustrating the steps of an embodiment of a method for forming an **SOI** structure according to the present invention;

Drawing Description Text - DRTX (4):
FIG. 13 is a plan view of the **SOI** structure formed by the method shown in FIGS. 1 to 12;

Drawing Description Text - DRTX (5):
FIGS. 14 to 17 are partial, cross-sectional views illustrating additional steps of an embodiment of the method for forming an **SOI** structure according to the present invention:

Drawing Description Text - DRTX (6):
FIG. 18 is a plan view of the **SOI** structure formed by the method shown in FIGS. 1 to 12 after the additional steps shown in FIGS. 14 through 17 have been performed;

Detailed Description Text - DETX (2):
FIG. 1 shows single crystal <100> silicon substrate 10 having all upper surface 12. Silicon substrate 10 is single crystalline as upper surface 12 will-later. act as a seed layer for epitaxial growth and to control etch characteristics during subsequent processing. In FIG. 2, first masking layer 20 has been formed on top of silicon substrate 10 and trenches 22 etched into

layer 20 exposing upper surface 12 of silicon substrate 10. First masking layer 20 may be formed, for example, by deposition of silicon oxide or silicon nitride. As shown in FIG. 3 trenches 30 have been etched in silicon substrate 10. Silicon trenches 30 include sidewalls 32 and bottom 34. Trenches 30 were formed by etching the silicon substrate with an anisotropic basic etch. When etched in strong bases, silicon in the <111> plane is not etched as readily as in the other planes, and sidewalls having an approximate slope of 35.degree. normal to the <100> plane will be formed. One suitable etchant is an aqueous solution of **tetramethylammonium** hydroxide. A solution of 450 grams of the pentahydrate salt dissolved per liter of water will have a lateral etch rate of 0.4 microns/minute at 65.degree. C. If trench 22 in first masking (layer 20 is 4000 angstroms wide and trench 30 etched 4000 angstroms deep, overhang 24 will be 650 angstroms. This overhang 24 allows the same photomask to be used at the next masking step. Other etchants that will produce similar preferential etching include 20% aqueous potassium hydroxide saturated with isopropanol at 80.degree. C. and ethylenediamine/pyrocatechol/water mixtures, both of which are well known to the industry. In FIG. 4, masking layer 20 has been removed, leaving silicon trenches 30 in silicon substrate 10.

Claims Text - CLTX (30):

15. The method according to claim 13, wherein said etchant is an aqueous solution of **tetramethylammonium** hydroxide, alcoholic potassium hydroxide, or aqueous ethylenediamine/pyrocatechol.